

1 / 13

FIG. 1

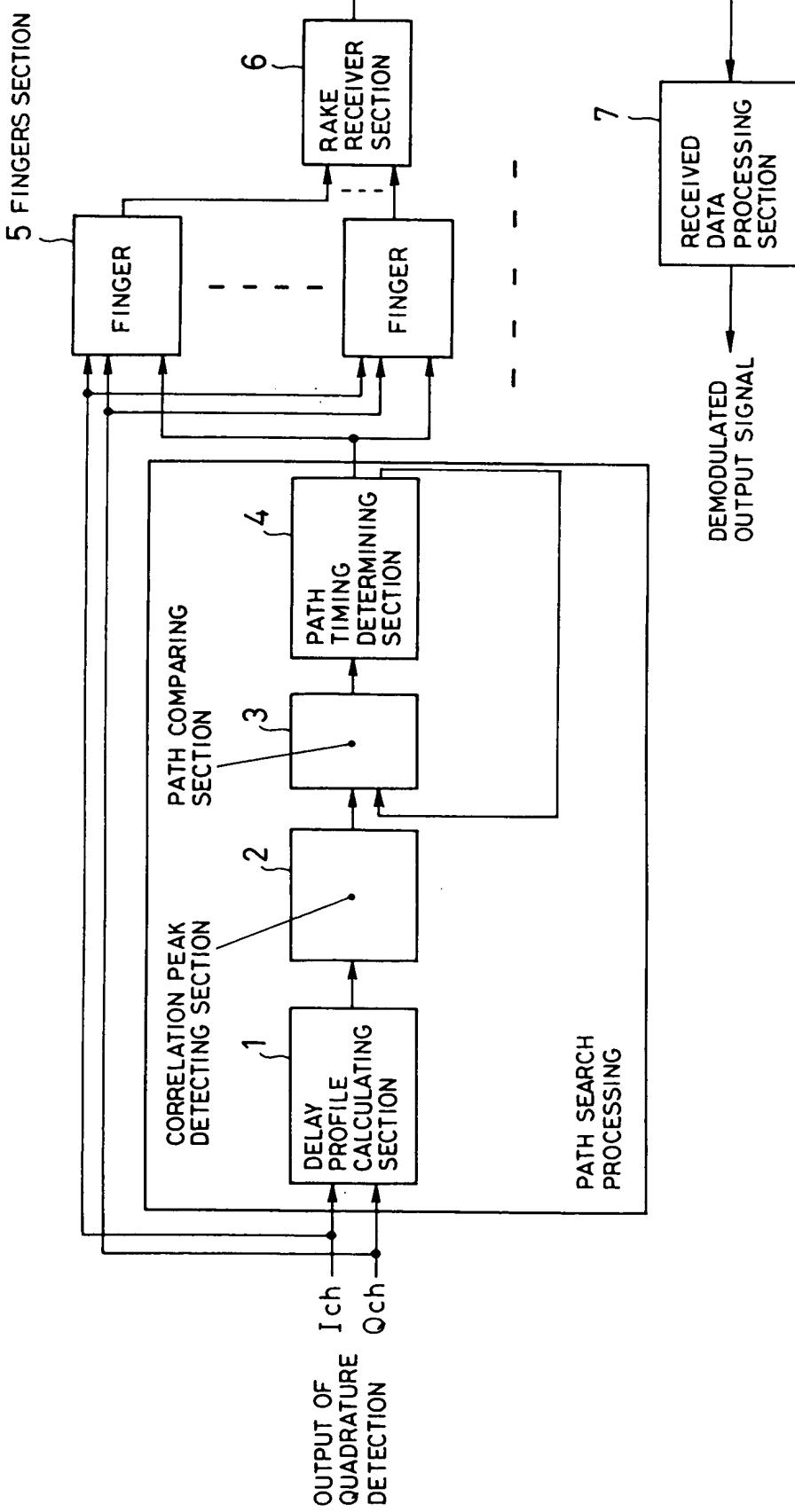


FIG. 2

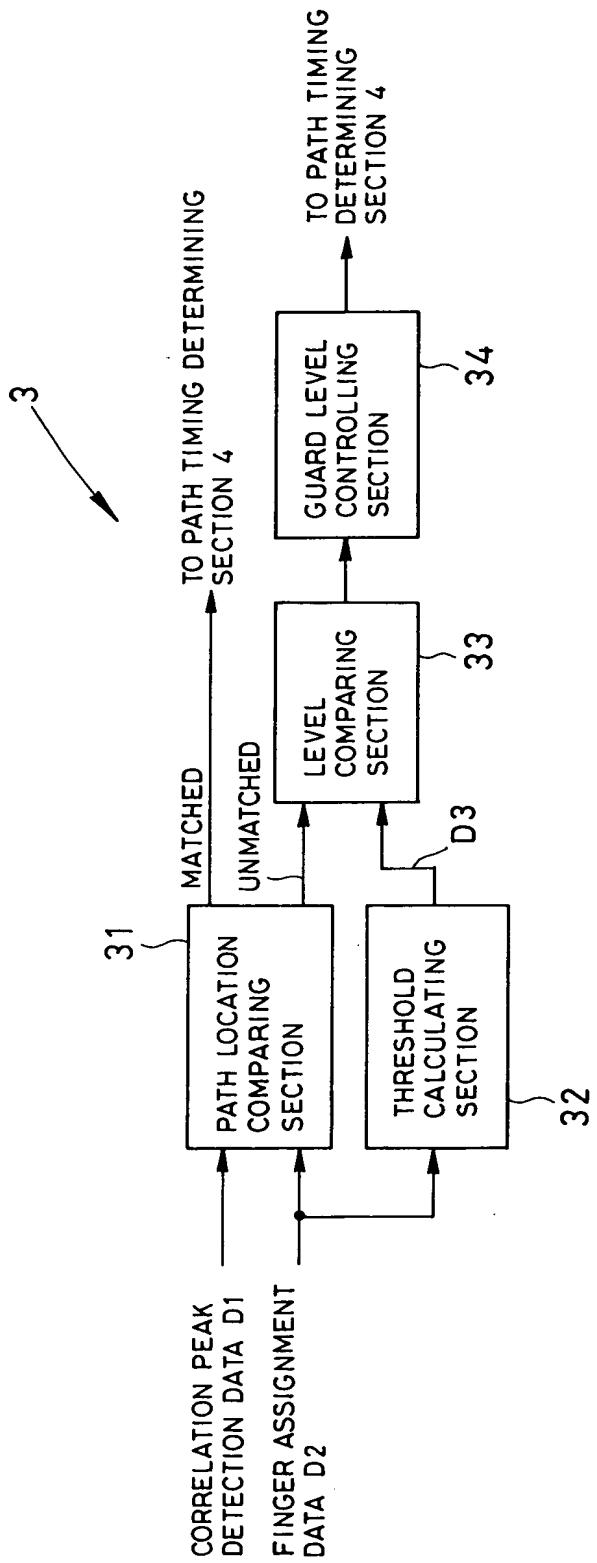


FIG.3

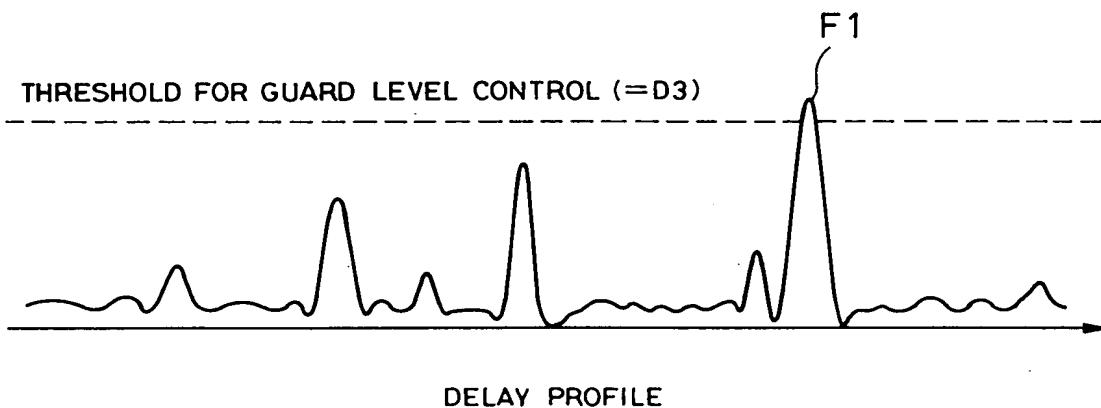
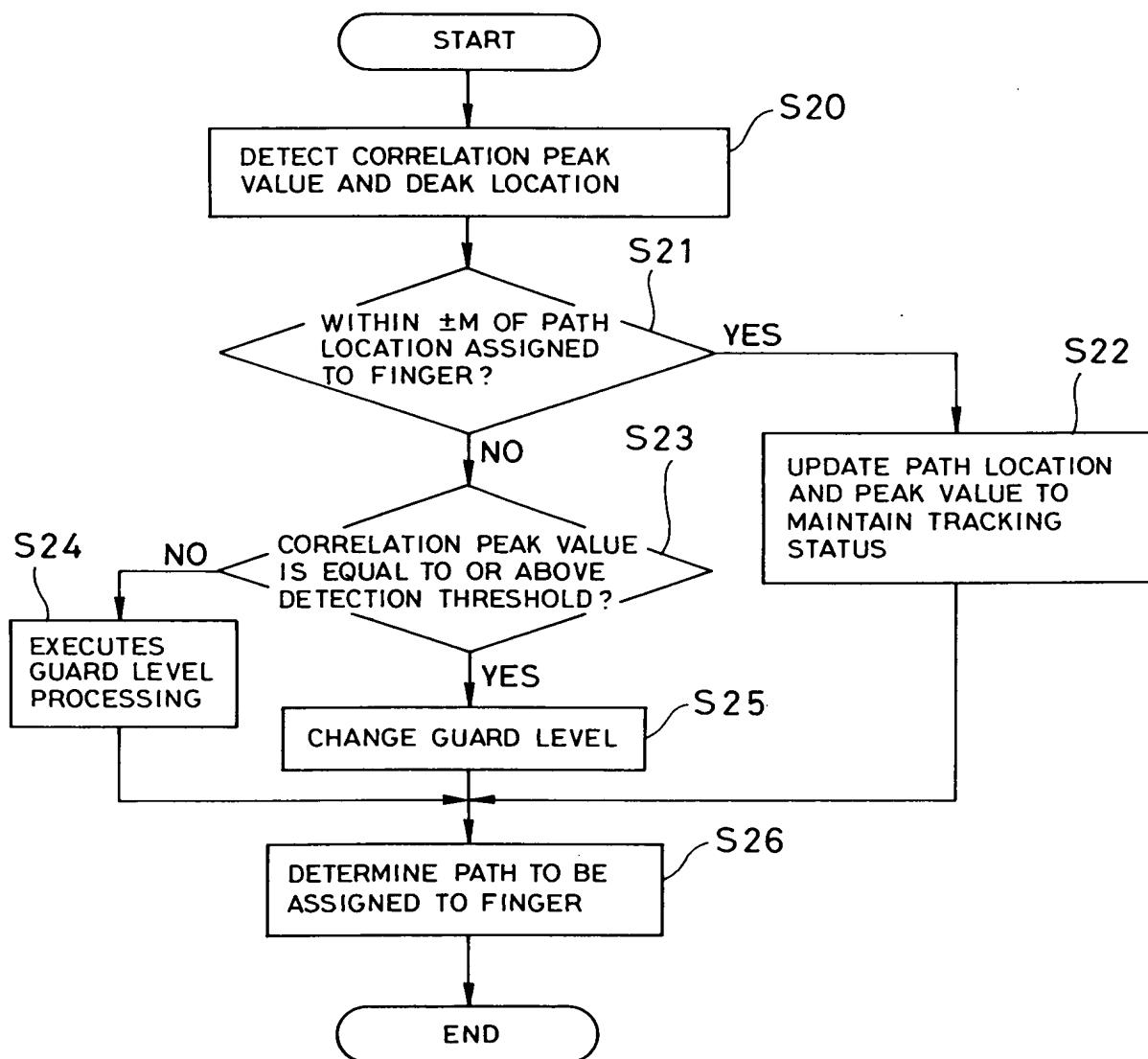


FIG. 4



5 / 13

FIG. 5

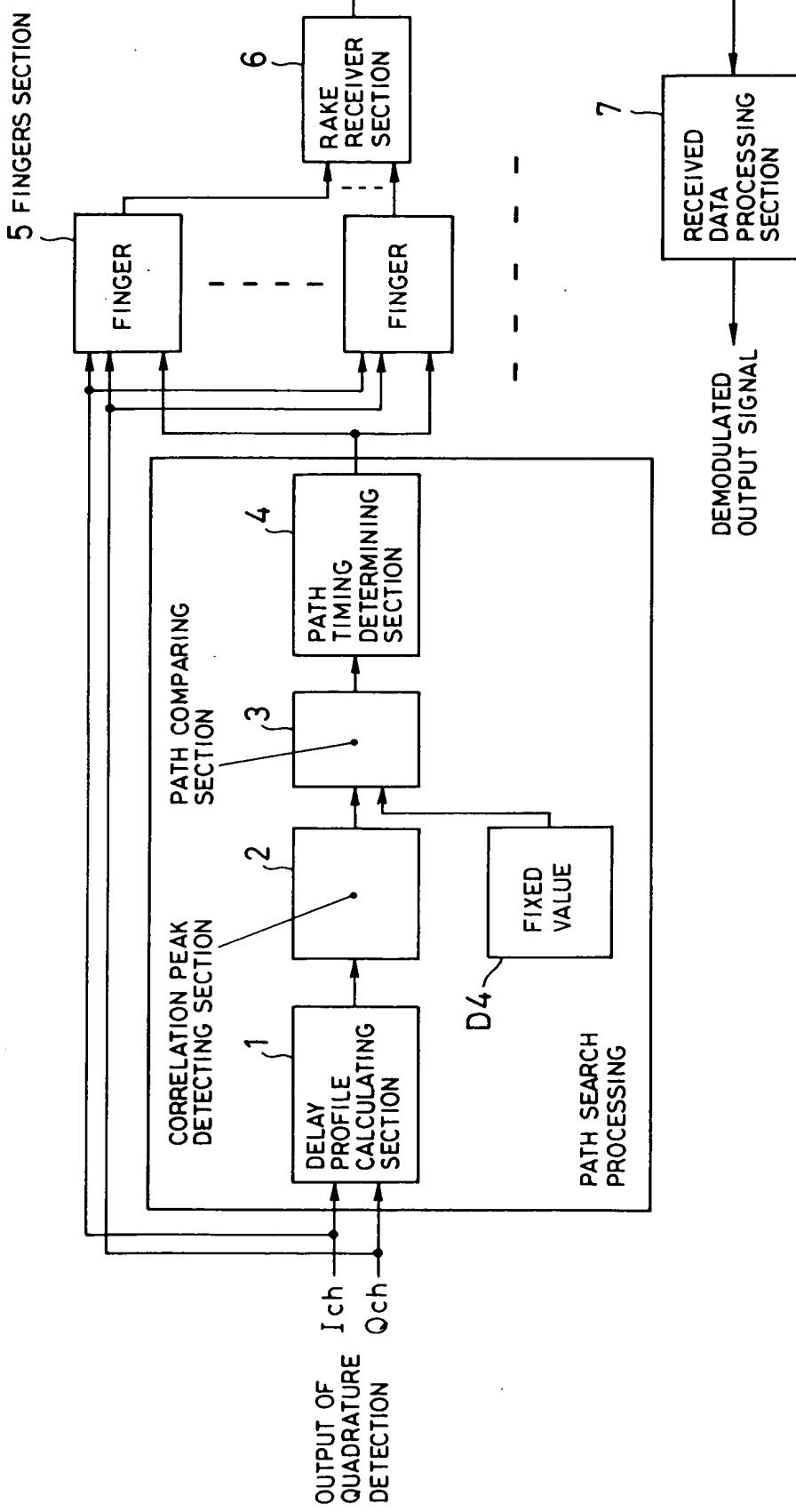
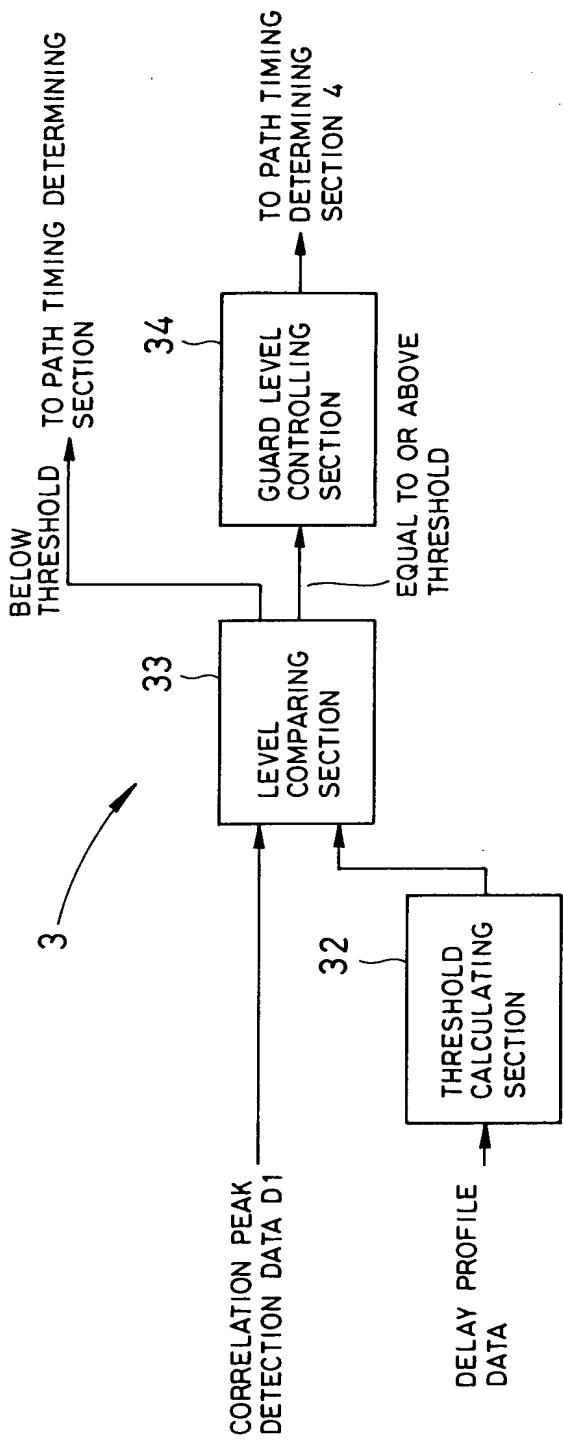


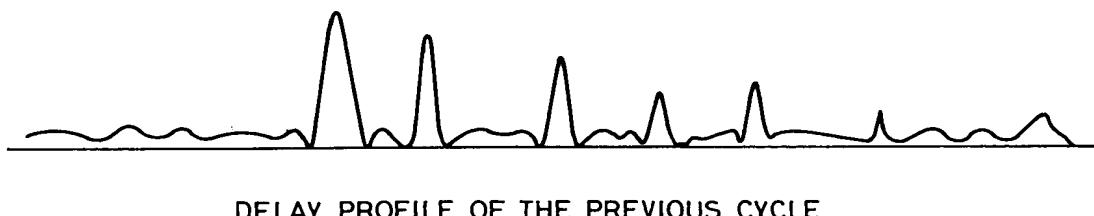
FIG. 6



7/13

FIG. 7

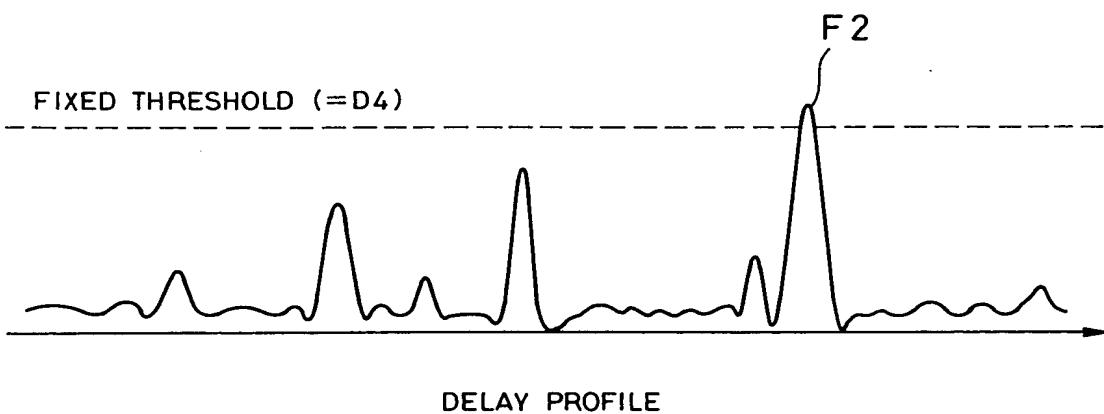
FIXED THRESHOLD (=D4)



DELAY PROFILE OF THE PREVIOUS CYCLE

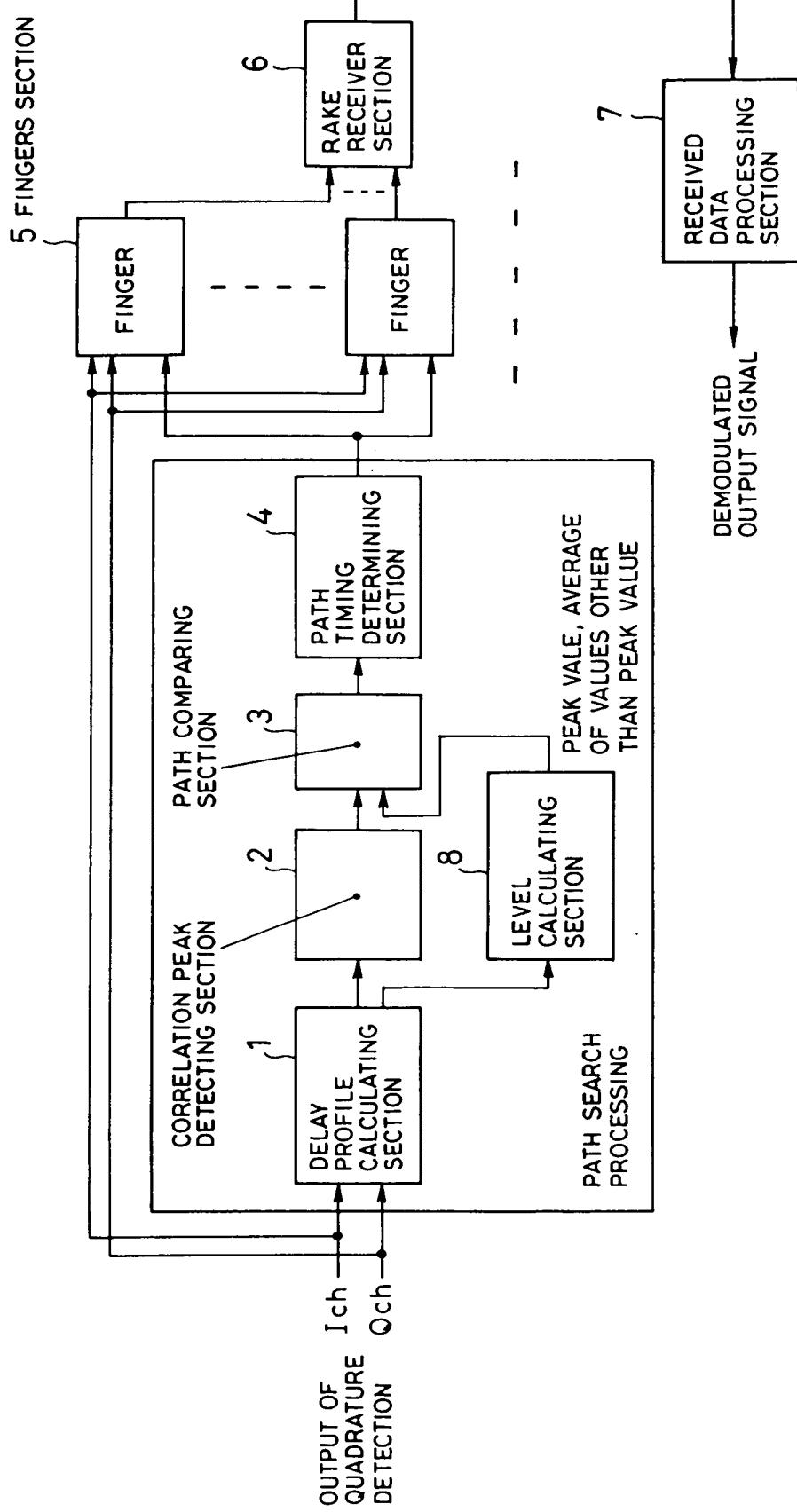
FIG. 8

FIXED THRESHOLD (=D4)



DELAY PROFILE

FIG. 9



9/13

FIG.10

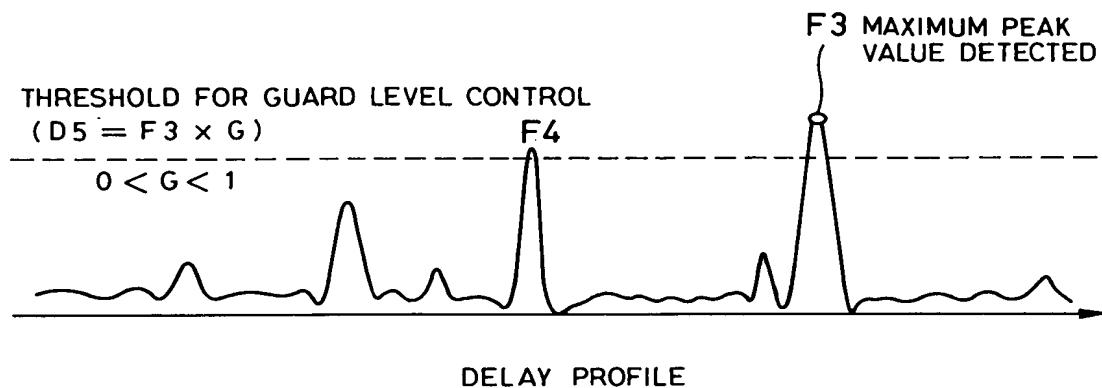


FIG.11

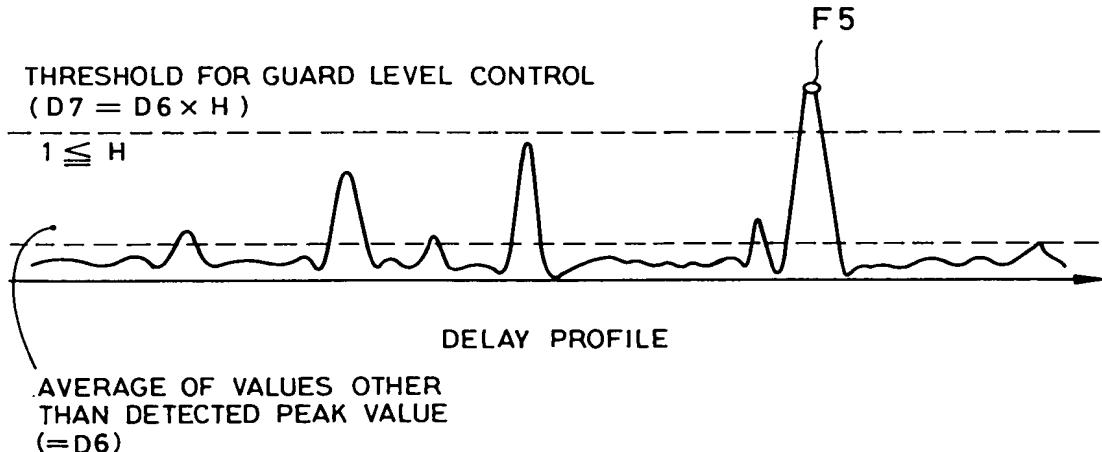
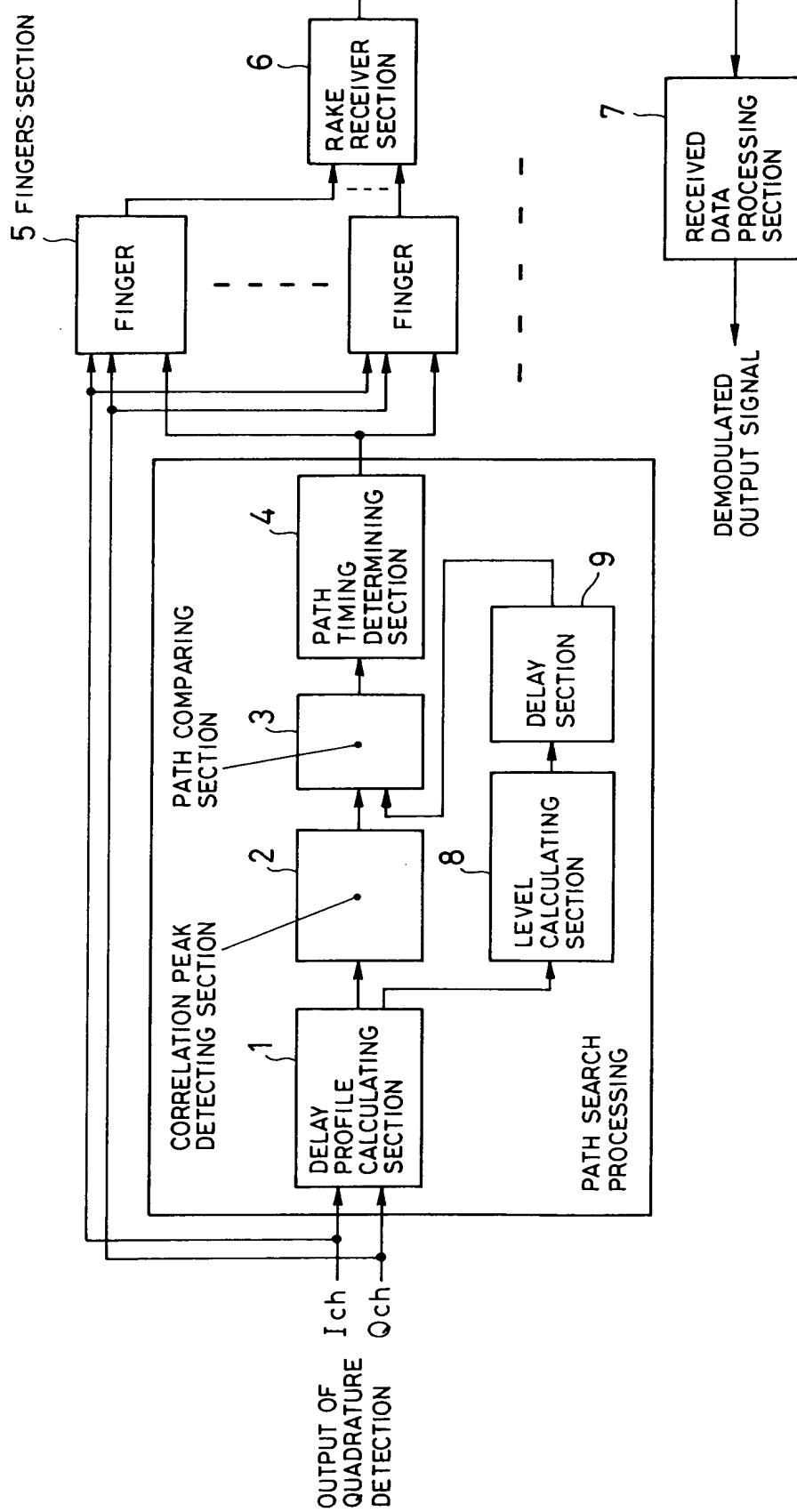


FIG. 12



11/13

FIG.13

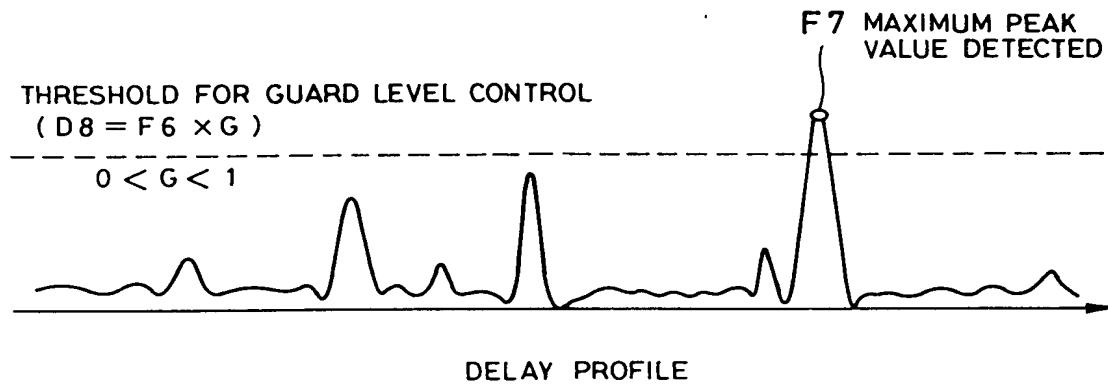


FIG.14

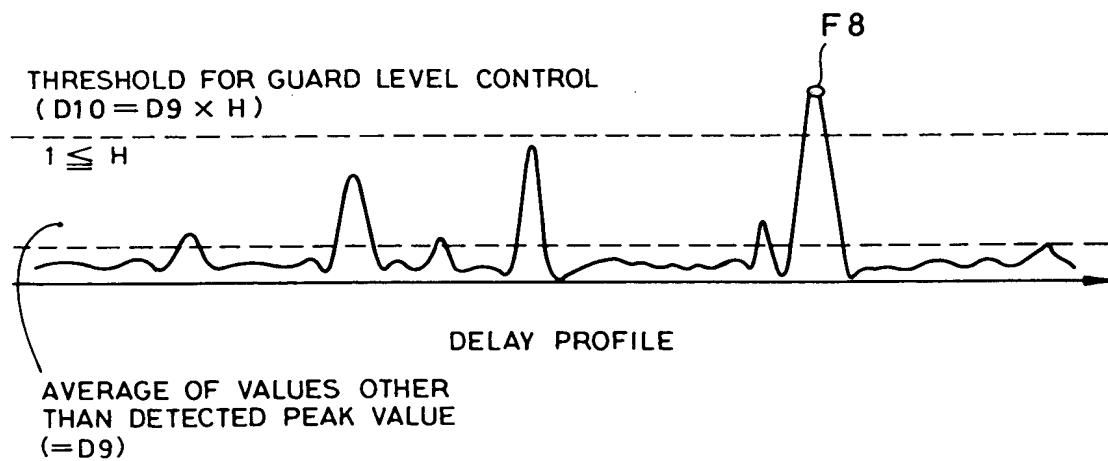
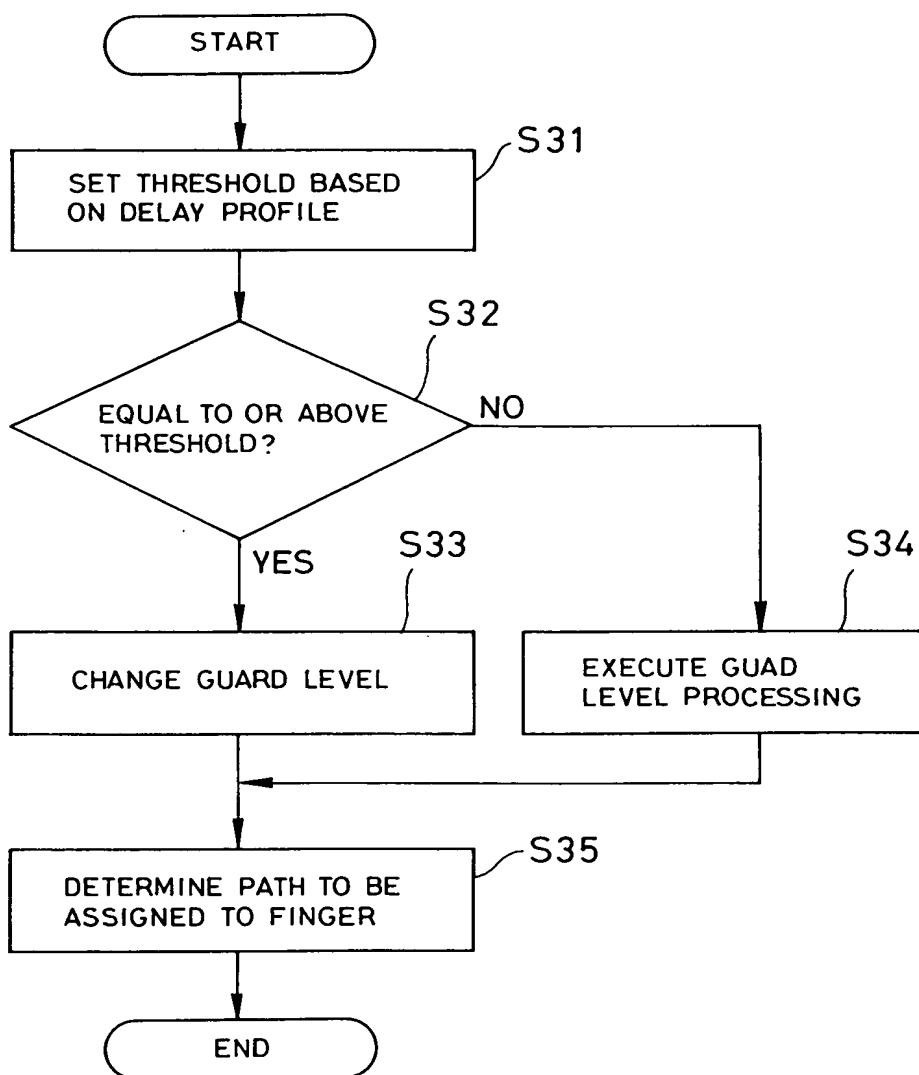


FIG.15



13/13

FIG.16

